

Review of multilevel inverter for high-power applications

Review of
MLIs

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Received 10 May 2023
Revised 3 June 2023
19 June 2023
19 August 2023
22 August 2023
Accepted 27 August 2023

Abstract

Purpose – Traditional level inverter technology has drawbacks in the aspect of Total harmonic distortion (THD) and switching losses for higher frequencies. Due to these drawbacks, two-level inverters have become unprofitable for high-power applications. Multilevel inverters (MLIs) are used to enhance the output waveform characteristics (i.e. low THD) and to offer various inverter topologies and switching methods.

Design/methodology/approach – MLIs are upgraded versions of two-level inverters that offer more output levels in current and voltage waveforms while lowering the dv/dt and di/dt ratios. This paper aims to review and compare the different topologies of MLI used in high-power applications. Single and multisource MLI's working principal and switching states for each topology are demonstrated and compared. A Simulink model system integrated using detailed circuit simulations in developed in MATLAB®–Simulink program. In this system, a constant voltage source connected to MLI to feed asynchronous motor with squirrel cage rotor type is used to demonstrate the efficacy of the MLI under different varying speed and torque conditions.

Findings – MLI has presented better control and good range of system parameters than two-level inverter. It is suggested that the MLIs like cascade-five-level and NPC-five-level have shown low current harmonics of around 0.43% and 1.87%, respectively, compared to two-level inverter showing 5.82%.

Originality/value – This study is the first of its kind comparing the different topologies of single and multisource MLIs. This study suggests that the MLIs are more suitable for high-power applications.

Keywords Multilevel inverters topologies, Inverters, Neutral point clamped, Active NPC, Neutral point piloted, Flying capacitor inverters, Cascaded H-bridge inverter

Paper type General review

1. Introduction

Inverters are DC-to-AC converters that use semiconductor switching devices to transfer electric energy parameter (i.e. voltage, current and/or frequency) at a desired value. Two-level inverters were introduced first. But the significant increase in the applications that requires DC-AC conversion has sparked the studies in inverter technologies (Balal *et al.*, 2022; Orfanoudakis *et al.*, 2010; Rahman and Saleh, 2011). However, two-level inverter soon became less-efficient for most of applications due to high total harmonic distortion (THD) in the output waveforms, switching losses and its limitations for medium voltage application due to dv/dt stress over semiconductor switches (Najafi and Yatim, 2011). To overcome these issues, higher switching frequency is used with a suitable filter to achieve output sinusoidal waveform. However, this will create a problem of switching losses



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Frontiers in Engineering and Built
Environment
Vol. 4 No. 2, 2024
pp. 77-89
Emerald Publishing Limited
e-ISSN: 2634-2502
p-ISSN: 2634-2499
DOI 10.1108/FEBE-05-2023-0020

(Balal *et al.*, 2022). Multilevel inverters (MLIs) are used to archive better performance using variety of techniques to overcome the limitations of two-level inverter. MLIs are upgraded versions of two-level inverters that offer more output levels in current and voltage waveforms while lowering the dv/dt and di/dt ratios. Depending on the supply type, such as current source inverters (CSIs) or voltage source inverters (VSIs), the output waveforms are produced as staircases of current or voltage. To obtain low THD, by increasing the number of voltage levels, a suitable topology is illustrated in Figure 1. Approximately, 28.88% of THD for three-level flying-capacitor MLI would be decreased to 18.56% with the use of five-level MLI of the same topology (Rana *et al.*, 2019). Also, it is shown that the two-level inverter with 1 kHz switching frequency generates 115% voltage THD, whereas MLIs develop only 22% and 32% voltage THD (Nordvall, 2011). With this significant difference between the two-level and multilevel techniques, MLI has been opted as the preferable one for many applications like renewable energy (solar/wind power inverters) up to megawatt (MW) power levels and motor-drive applications (Abd Halim *et al.*, 2016). The advantages of MLI are listed as:

- (1) Superior efficiency due to lower switching frequencies.
- (2) MLI enhances power quality and dynamic stability for the connected utilities.
- (3) Lower switching stress over the semiconductors.
- (4) Because to its modular and straightforward design, they can be built up to virtually infinite levels.
- (5) MLI can be considered as an ideal interface between the utilities and renewable energy sources (Balal *et al.*, 2022; Najafi and Yatim, 2011; Abd Halim *et al.*, 2016).

A comparison between the conventional two-level inverter and MLI is presented in Table 1 (Suresh, 2016).

Table 2 illustrates the resulted THD for conventional two-level and MLIs (Nordvall, 2011).

This paper aims to present an overview of different MLI schemes to identify the pros and cons of each topology. To identify the efficacy of the MLI, a model for MLI with Induction Motor drive (IM) in MATLAB Simulink is developed. At different speed and torque

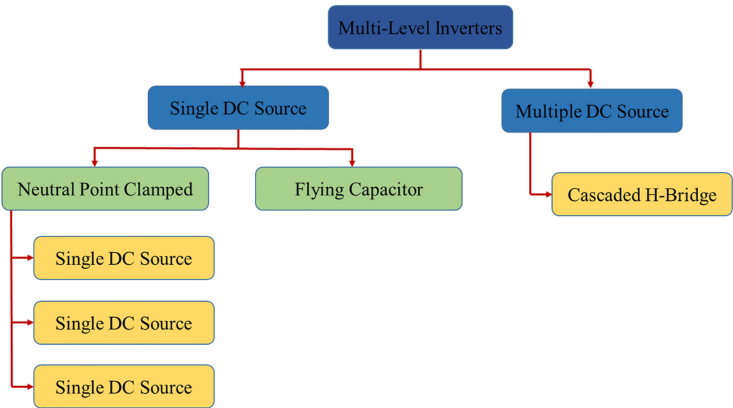


Figure 1.
Classification of
multilevel inverters

Source(s): Figure courtesy of Wu and Narimani (2017a, b)

variations, the voltage and current THD responses are obtained and analyzed to demonstrate the inverter performance at different loads.

2. Topologies of multilevel inverter

There are two types of MLIs based on the number of voltage sources utilized to feed the MLIs as follows (Wu and Narimani, 2017a; Akagi, 2019):

- (1) Single DC source.
- (2) Multiple DC source.

A single voltage source is divided into a number of capacitors to acquire different voltage levels, whereas the second type requires different sources of voltage, whether from multiple batteries or through separate convertor rectifiers linked to renewable energy sources or many others. The classification of MLI is presented in Figure 1.

2.1 Multiple DC source

The MLI topology that uses multiple voltage supplies is cascaded H-bridge (Saleh and Rahman, 2011). This topology uses multiple units of identical H-bridge power cells connected in a series chain to produce high ac voltages. Each power cell is connected to separate and equal DC voltage supply. Advantages can be obtained from the modular structure contributes to low production costs. Also, redundant switching patterns can be achieved, which provides flexibility in switching design. Moreover, this topology can be extended to infinite number of levels to meet the required standard for the output waveform. However, one of the defining shortcomings of this technology is the significant need for separate voltage sources to power the cells (Wu and Narimani, 2017a; Shehu *et al.*, 2016). A five-level CHB inverter is shown in Figure 2 with its switching pattern in Table 3. It consists of two H-bridge cells per phase.

S. No.	Two-level inverter	Multilevel inverter
1	Output waveform contains higher THD	Low THD in the output waveform
2	Larger switching stress	Low switching stress
3	It has limitation with high voltage applications	Can be used for high voltage applications
4	Cannot produce high voltages	It can produce high voltage levels
5	Larger dv/dt	Low dv/dt
6	Increased switching losses due to higher switching frequency	Reduced switching losses because of lower switching frequency

Source(s): Table courtesy of Suresh (2016)

Table 1.
Comparison of two-level inverter and multilevel inverter

Topology	Two-level	Cascaded five-level	NPC-five-level
Voltage THD% @ 1kHz	114.95	29.65	31.57
Current THD% @ 1kHz	5.82	0.43	1.87

Source(s): Table courtesy of Nordvall (2011)

Table 2.
THD value for the two-level, cascaded five-level, and NPC-five-level inverter

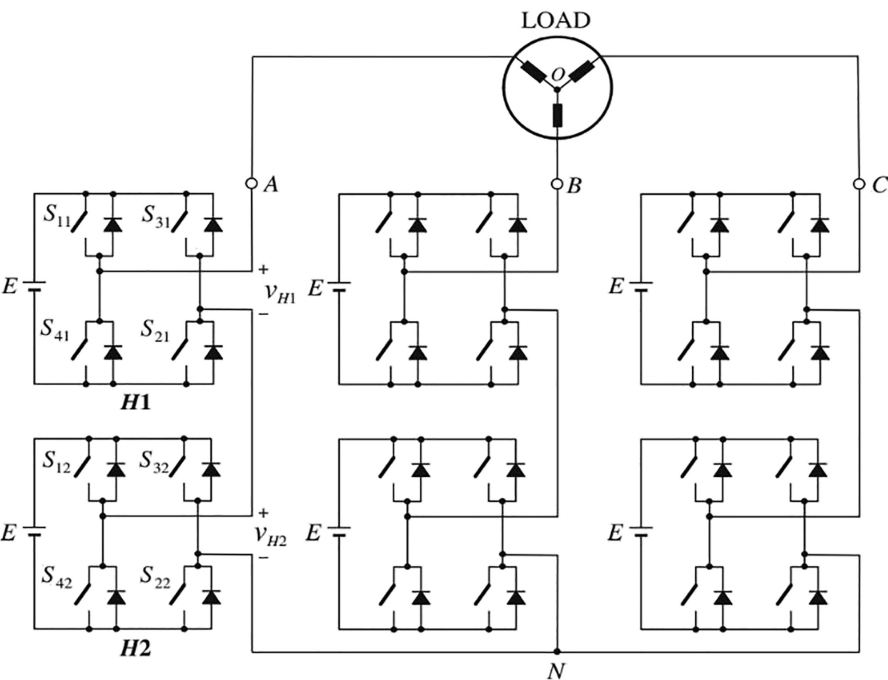


Figure 2.
5-Level cascaded
H-bridge inverter

Source(s): Figure courtesy of Saleh and Rahman (2011)

Output voltage V_{AN}	S_{11}	Switching state		S_{32}	V_{H1}	V_{H2}
		S_{31}	S_{12}			
$2E$	1	0	1	0	E	E
	1	0	1	1	E	0
E	1	0	0	0	E	0
	1	1	1	0	0	E
0	0	0	1	0	0	E
	0	0	0	0	0	0
	0	0	1	1	0	0
	1	1	0	0	0	0
	1	1	1	1	0	0
	1	0	0	1	E	$-E$
$-E$	0	1	1	0	$-E$	E
	0	1	1	1	$-E$	0
	0	1	0	0	$-E$	0
	1	1	0	1	0	$-E$
$-2E$	0	0	0	1	0	$-E$
	0	1	0	1	$-E$	$-E$

Table 3.
Five-level CHB inverter
switching states

Source(s): Table courtesy of Elbarbary

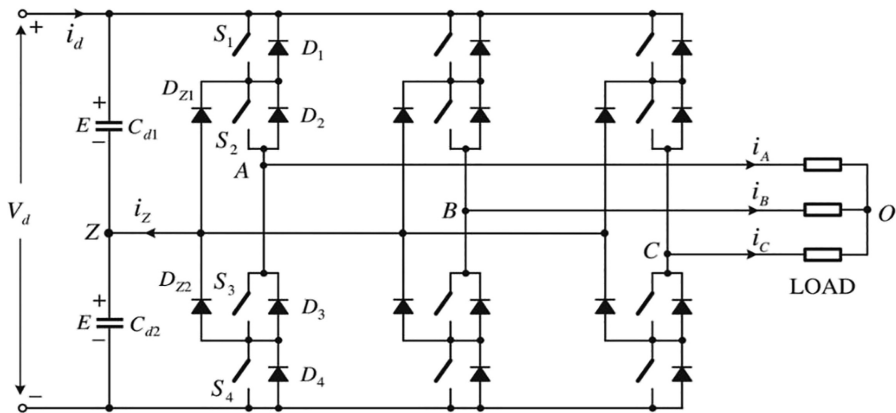
2.2 Single DC source

As per above map, single DC supply MLIs is divided as follows.

2.2.1 *Neutral point clamped (NPC-MLI)*. Single voltage source is utilized in neutral point clamped MLIs and is split into several capacitors linked in series according to the appropriate number of voltage levels. We shall divide the source into $x - 1$ capacitors that are linked to the source in series to get x levels. Figure 3 presents three-level NPC-MLI where the neutral point between the two feeding capacitors (i.e. point z) can be accessed through two clamping diodes. It is most suitable for high-power MV drives with advantages such as the reduced dv/dt and THD for the resultant waveform and, also, the applied voltage is equal on all switching devices in the commutation mode, whereas the drawbacks consider additional clamping diodes for high order of levels, asymmetrical power losses in the switching devices and the necessity of control loop for neutral point voltage deviation (Rana *et al.*, 2019; Nordvall, 2011; Abd Halim *et al.*, 2016; Wu, 2006; Young *et al.*, 2012). Switching pattern is illustrated in Table 4.

2.2.2 *Active neutral point clamped MLI (ANPC)*. This kind of frequency inverter was developed to address one of the drawbacks of the NPC, namely the uneven distribution of losses in the switches, which results in an insufficient distribution of heat inside them. Switches 5 and 6 in Figure 4, for example, control and balance the loads on the switches. However, the entire converter system becomes more expensive and complicated when active clamping switches are used. Table 5 indicates the switching pattern for the three voltage levels.

2.2.3 *Neutral point piloted MLI (NPP)*. Bidirectional switches are added between the inverter output terminals and the dc bus neutral point to create the NPP inverter topology,



Source(s): Figure courtesy of Rana *et al.* (2019)

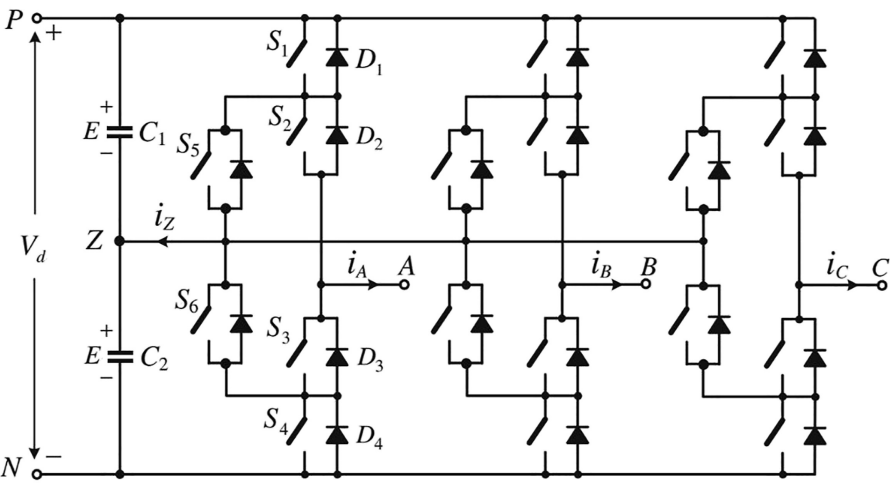
Figure 3.
Three-level multilevel
DC-MLI

Switching state	Device switching status (phase A)				Inverter terminal voltage V_{AZ}
	S_1	S_2	S_3	S_4	
P	On	On	Off	Off	E
O	Off	On	On	Off	0
N	Off	Off	On	On	$-E$

Source(s): Table courtesy of Rana *et al.* (2019)

Table 4.
Switching states of
DC-MLI

Figure 4.
Active neutral point
clamped MLI



Source(s): Figure courtesy of El-Hosainy *et al.* (2017)

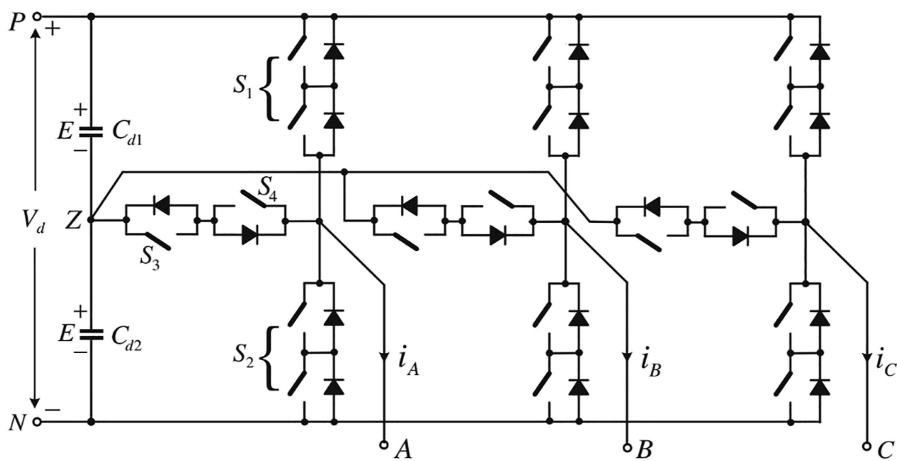
Table 5.
Switching states for
active neutral point
clamped MLI

Switching state		Switching states (phase A)						Inverter voltage V_{AZ}
		S_1	S_2	S_3	S_4	S_5	S_6	
P		1	1	0	0	0	1	E
O	OU ₁	0	1	0	0	1	0	0
	OU ₂	0	1	0	1	1	0	
	OL ₁	0	0	1	0	0	1	
	OL ₂	1	0	1	0	0	1	
N		0	0	1	1	1	0	−E

Source(s): Table courtesy of El-Hosainy *et al.* (2017)

which is evolved from the two-level inverter. As a result, the dv/dt and THD of the three-level voltage waveforms produced by this inverter are minimized. But there are certain restrictions with the NPP inverter where each switch position on the inverter requires a series connection of two or more switches depending on the potential rating. This questions the reliability and complexity of the system. Figure 5 shows three-level NPP inverter, and Table 6 indicates its switching states (Orfanoudakis *et al.*, 2010; Wu and Narimani, 2017b; Guennegues *et al.*, 2009).

2.2.4 Flying-capacitor MLI (FLC-MLI). Figure 6 displays a 5L-FLC arrangement. This inverter is a two-level inverter with cascaded dc capacitors. Each inverter leg contains three flying capacitors with voltage ratings of $3E$, $2E$ and E ($E = V_d / 4$). Inverter legs have four switch pairs. Four gate signals are needed for an inverter leg's eight switches. The main features considered are the modular structure of the switches as well as reduced THD and dv/dt . However, this topology requires numerous dc capacitors equipped with precharging circuits and, also, inverter operating conditions affect flying capacitor voltages. To minimize dc voltage deviation concerns, flying capacitor voltages must be precisely regulated, increasing control system complexity. Because of the aforesaid disadvantages, flying-capacitor inverter's practical usage in MV drives is restricted. However, this inverter topology may be utilized to derive sophisticated converter topologies. Table 7 explains the



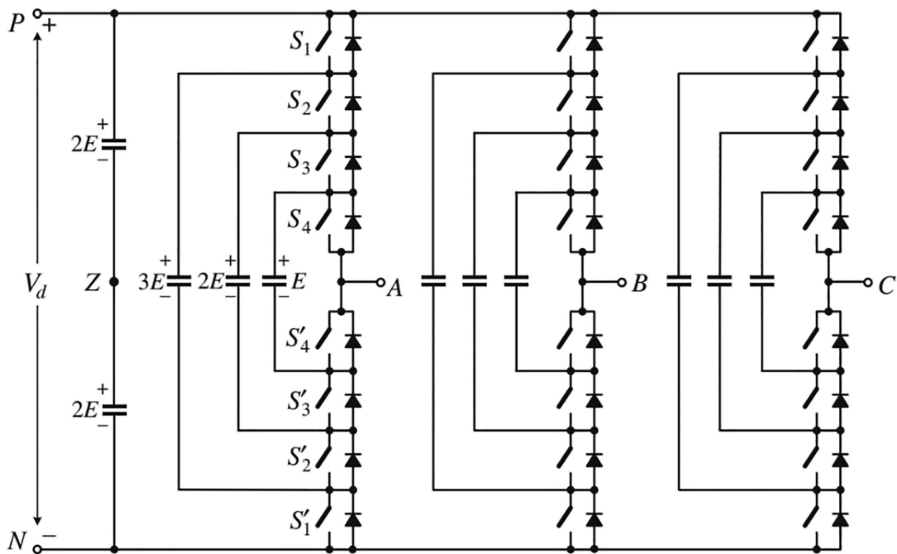
Source(s): Figure courtesy of Orfanoudakis *et al.* (2010)

Figure 5.
Neutral point
piloted MLI

Switching state	Switching state (phase A)				Inverter phase Voltage V_{AZ}
	S_1	S_2	S_3	S_4	
[P]	1	0	1	0	E
[O]	0	0	1	1	0
[N]	0	1	0	1	-E

Source(s): Table courtesy of Orfanoudakis *et al.* (2010)

Table 6.
Switching states for
NPP-MLI



Source(s): Figure courtesy of Rana *et al.* (2019)

Figure 6.
5-Level flying-
capacitor MLI

Table 7.
Switching states for
5L-multilevel FLC
inverter

Switching state (phase A)					Inverter phase voltage V_{AZ}
S_1	S_2	S_3	S_4		
1	1	1	1		2E
1	1	1	0		E
0	1	1	1		
1	0	1	1		
1	1	0	1		
1	1	0	0		0
0	0	1	1		
1	0	0	1		
0	1	1	0		
1	0	1	0		
0	1	0	1		
1	0	0	0		−E
0	1	0	0		
0	0	1	0		
0	0	0	1		
0	0	0	0		−2E

Source(s): Table courtesy of [Rana et al. \(2019\)](#)

switching pattern for 5L-FLC inverter ([Rana et al., 2019](#); [Nordvall, 2011](#); [Akagi, 2019](#); [Shehu et al., 2016](#); [Wu and Narimani, 2017b](#); [El-Hosainy et al., 2017](#)).

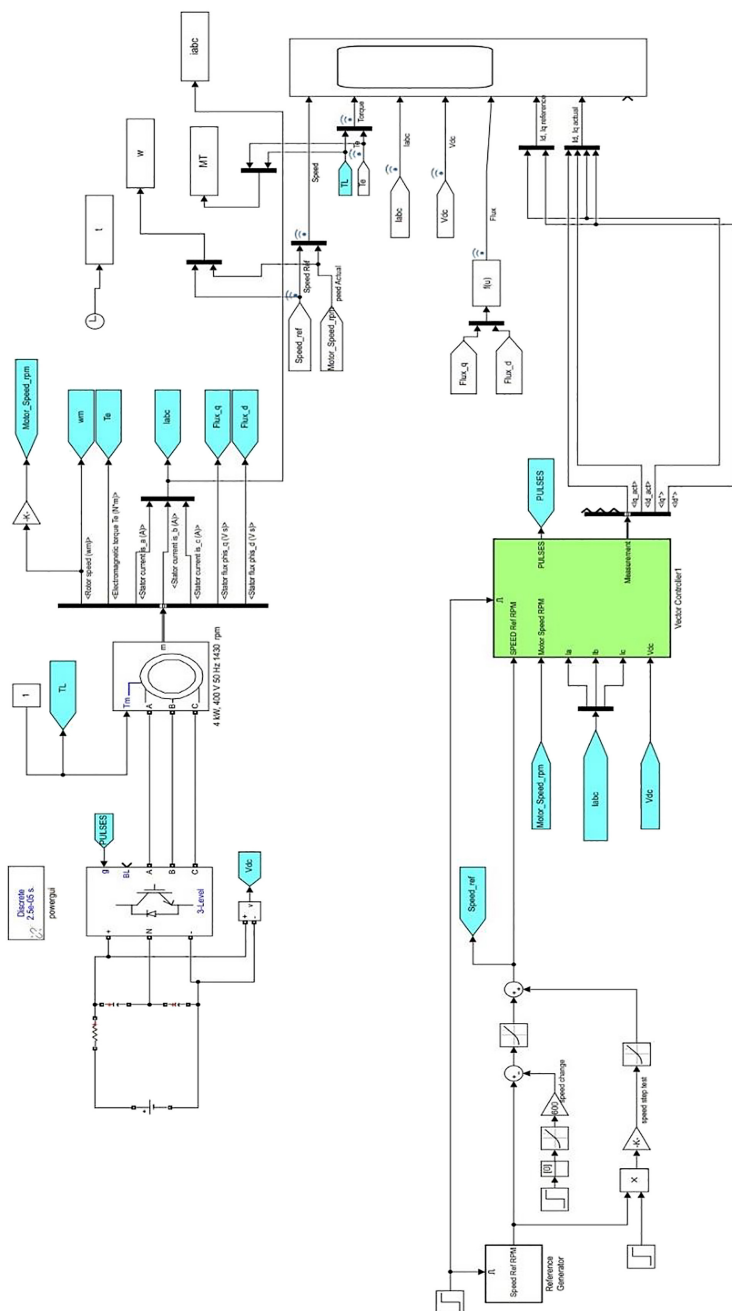
[Table 8](#) presents the comparison of consolidated features of the different MLI topologies discussed in this paper ([Suresh, 2016](#); [Hoon et al., 2017](#); [Lai and Peng, 1996](#);

Table 8.
Comparison of features
of different multilevel
inverter topologies

S. No.	Topology	Neutral point diode clamped	Flying capacitor	Cascaded H-bridge
1	DC link	$(n - 1)$	$(n - 1)$	$3(n - 1)/2$
2	Capacitors			
2	Switches with freewheeling diodes	$6(n - 1)$	$6(n - 1)$	$6(n - 1)$
3	Clamping Diodes	$3(n - 1)(n - 2)$	0	0
4	Clamping Capacitors	0	$3(n - 1)(n - 2)/2$	0
5	Voltage Unbalancing	Average	High	Very Small
6	Advantages	sturdy design and uses the least quantity of DC-link capacitors necessary (less voltage imbalance problems)	Voltage balancing of DC-link capacitors can be accomplished using phase redundancy	Due to its modularity, it has an easy structure and control
7	Disadvantages	Increased number of clamping diodes with the increasing number of levels	Bulky size and more costly with more complex voltage balancing control algorithms	Requires multiple separate DC sources
8	Applications	Motor Drive System, STATCOM	Motor Drive System, STATCOM	Motor Drive System, PV, Fuel cells, Battery system

Source(s): Table courtesy of [Hoon et al. \(2017\)](#)

Simulation results



Source(s): Figure courtesy of Elbarbary (2023)

Figure 7.
Simulink model of
multilevel inverter to
feed squirrel cage
induction motor

3. Simulation results

A model system integrated using detailed circuit simulations in MATLAB®–Simulink program. In this system, a constant voltage source connected to MLI was used to feed Asynchronous motor with squirrel cage rotor type as shown in Figure 7.

Speed reference was applied on the motor with step changes. Also, the values of the reference torque were stepped up from no load to the maximum torque, and this allows to examine the MLI under various conditions and to verify the response of the motor currents. Figure 8, illustrates the speed and torque reference values for this model.

Figure 9 shows the source voltage response along with the motor three phase currents, speed and torque. It is observed that when the speed is increased, the motor draws larger instantaneous currents, which is reflected in the MLI.

4. Conclusion

With the innovation and growth of industrial sectors on a global and local scale, the need for high-energy converters continues to rise. Increase in significance and demand of MLIs for both low- and high-power applications are observed. This article describes and presents five types of MLI topologies (Rodrí *et al.*, 2007). It is suggested that the MLIs like cascade-five-level and NPC-five-level have shown low current harmonics of around 0.43% and 1.87%, respectively, than two-level inverter showing 5.82%. In order to reduce the number of power switches in multilayer inverters, it is possible to reduce or rearrange the DC input voltages, according to the assessment. Other than that numerous academicians have presented specific topological explanations and resolutions in consideration of the desired use.

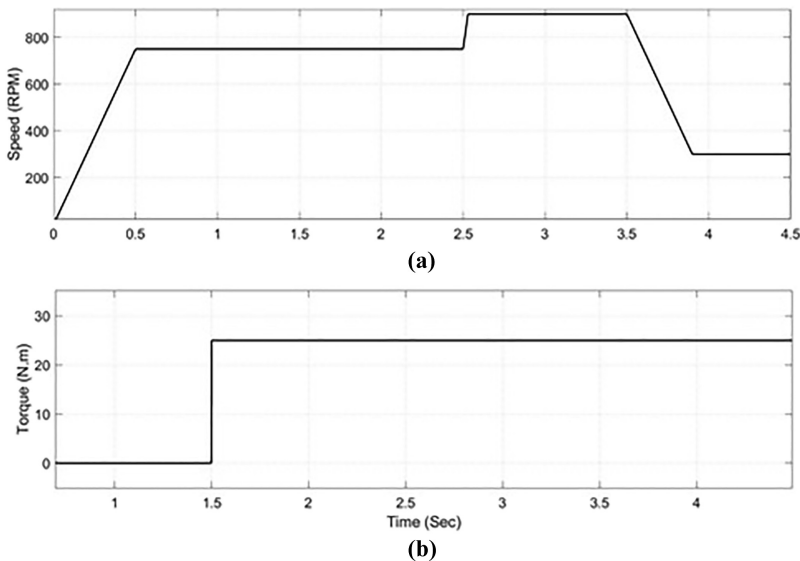


Figure 8.
(a) Speed reference and
(b) torque references
for the IM

Source(s): Figure courtesy of Elbarbary (2023)

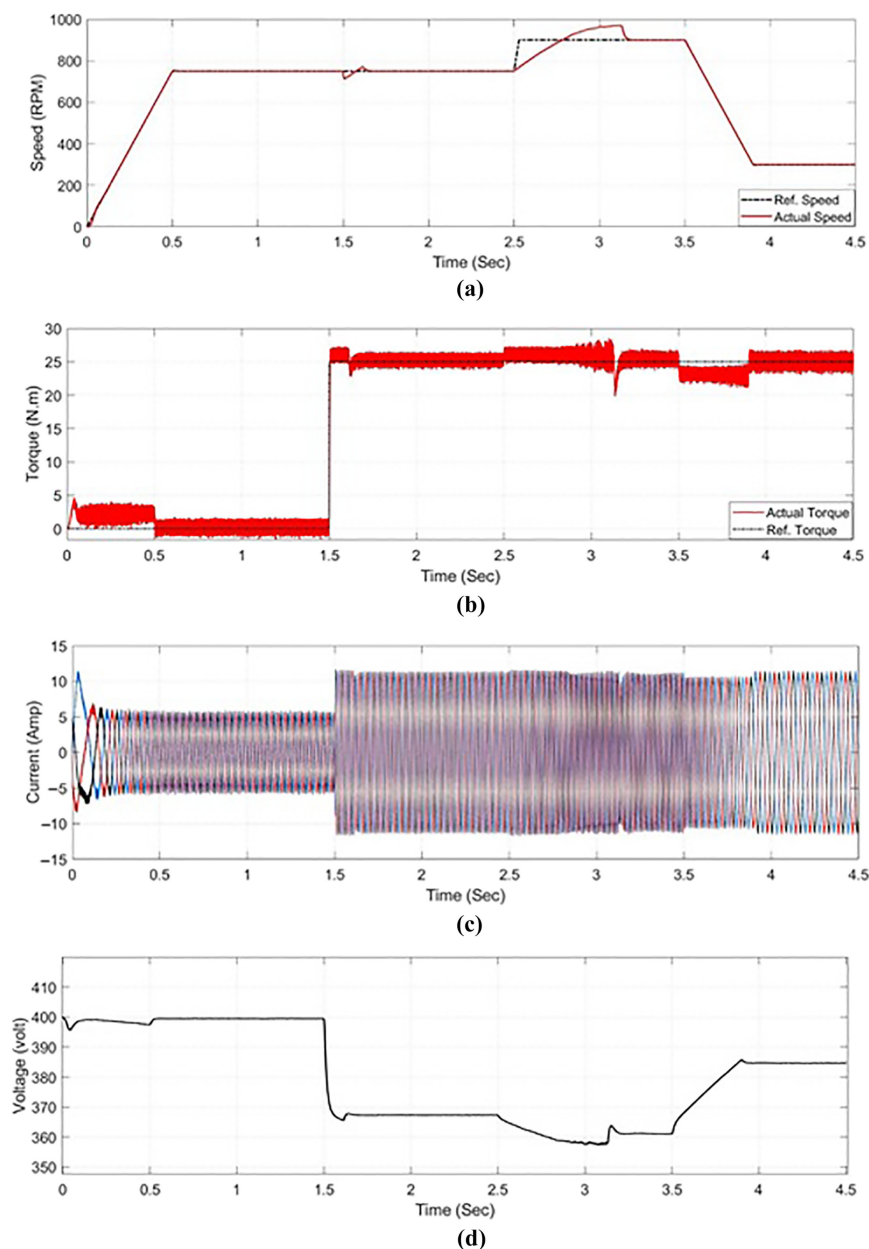


Figure 9.
(a) Actual speed, (b)
actual torque, (c) three-
phase motor currents
and (d) DC source
performance

Source(s): Figure courtesy of Elbarbary (2023)

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